EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	(check$4 determin$4 verif$4) with floating with rotating adj registers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:14
L2	4	(check$4 determin$4 verif$4) same floating with rotating adj registers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:14
L3	19	static adj register with rotating adj registers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:14
L4	8	loop same (rotating adj register) same (spill$4 fill$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:15
L5	12	pipe$line with (rotating adj register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:16
L9	52	pipe$line same floating same register same loop	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:16
L10	17	pipe$line same (rotating adj register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:17
L11	65	loop same (rotating adj register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:18

EAST Search History

S1	2	"6651247".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/23 14:22
S2	14	(spill$4 with fill$4) with register with address	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/23 14:27
S4	27	(check$4 determin$4 verif$4) with rotating adj registers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:13

Sign in

Google

Web Images Video[New!] News Maps more »

rotating register spill fill Search Advanced Search Preferences

Web

Results 1 - 10 of about 207,000 for rotating register spill fill. (0.35 seconds)

[PDF] Microsoft PowerPoint - 2_robert
File Format: PDF/Adobe Acrobat - View as HTML
Restore scratch. **Spill** r2. **Fill** r2. Dynamic shrink wrapping: ... **Register Spill** Problems. • no compiler cooperation. – **Rotating register** files ...
rogue.colorado.edu/EPIC4/presentations/2_robert_6pclr.pdf - Similar pages

The Intel IA-64 Compiler Code Generator
These include not-a-thing (NaT) bit maintenance during **spill/fill**, advanced load ... After modulo scheduling and **rotating register** allocation,12 LC, EC, ...
doi.ieeecomputersociety.org/10.1109/40.877949 - Similar pages

[PDF] TI IA-64 CCG
File Format: PDF/Adobe Acrobat - View as HTML
spill/fill, advanced load address table (ALAT). awareness for data-speculative registers, cor-. rect **rotating register** allocation for the soft- ...
www.gelato.org/pdf/Workshops/geneva05/icc_generator_2000_intel.pdf - Similar pages

[PDF] Intel Itanium Architecture Basics Cameron McNairy Itanium ...
File Format: PDF/Adobe Acrobat - View as HTML
Register Stack. Alloc sets the frame region to the desired size. Three architecture parameters: local, output, and **rotating**. Avoids **register spill/fill** upon ...
www.gelato.org/pdf/apr2006/gelato_ICE06apr_itanium101_mcnairy_intel.pdf - Similar pages

[PPT] IA-64 Architecture Innovations
File Format: Microsoft Powerpoint - View as HTML
Automatic save/restore of GRs on procedure call/return; Cache traffic reduction; Latency hiding of **register spill/fill**. General Registers. Stacked ...
www.es.ele.tue.nl/~heco/courses/aca/IA64/dale.ppt - Similar pages

Methods and apparatus for efficient control of floating-point ...
The **rotating register** permits multiple iterations of the program loop to be ... **Spill/fill** operations may be performed, for example, when a program is ...
www.freepatentsonline.com/6151669.html - 81k - Cached - Similar pages

[PDF] Prematerialization: Reducing **Register** Pressure for Free
File Format: PDF/Adobe Acrobat - View as HTML
and **rotating** is irrelevant. Therefore, there is no need for ... processor is stalled waiting for a **register** window to **spill/fill** can ...
www.cs.virginia.edu/~pact2006/program/pact2006/pact146-baev2.pdf - Similar pages

[PDF] Rapid Development of a Flexible Validated Processor Model
File Format: PDF/Adobe Acrobat - View as HTML
return values reminiscent of the **rotating register** windows ... and inserts implicit **register spill** and **fill** instructions. The ...
liberty.princeton.edu/Publications/mobs05_i2.pdf - Similar pages

IA-64 - Wikipedia, the free encyclopedia
Rather than the typical **spill/fill** or window mechanisms used in other processors, the Itanium processor can **rotate** in a set of new registers to accommodate ...
en.wikipedia.org/wiki/IA-64 - 27k - Cached - Similar pages

[PDF] Ten Hardware Features That Affect Optimization

File Format: PDF/Adobe Acrobat - View as HTML
Background engine performs **fill** and **spill** operations on. **register** stack ... **Register** Stack.
x86 Floating-point registers are organized as a **rotating** stack ...
www.cs.rice.edu/~keith/512/Lectures/Hardware-4up.pdf - Similar pages

Gooooooooogle ▶
Result Page: 1 2 3 4 5 6 7 8 9 10 **Next**

rotating register spill fill Search

Search within results | Language Tools | Search Tips | Dissatisfied? Help us improve

Google Home - Advertising Programs - Business Solutions - About Google

Sign in

Google

Web Images Video[New!] News Maps more »

rotating register spill Search | Advanced Search Preferences

Web

Results **1** - **10** of about **215,000** for **rotating register spill**. (**0.40** seconds)

[PDF] Microsoft PowerPoint - 2_robert
File Format: PDF/Adobe Acrobat - View as HTML
Optimal **spill** placement is less important. 16. **Register Spill** Problems. • no compiler cooperation. – **Rotating register** files. – ALAT for data speculation ...
rogue.colorado.edu/EPIC4/presentations/2_robert_6pclr.pdf - Similar pages

Citations: **Register** allocation for software pipelined loops - Rau ...
Once the **register** allocation and **spill** is completed for R1, the algorithm ... Because this specific case of **rotating register** file allocation and ordinary ...
citeseer.ist.psu.edu/context/34277/0 - 81k - Cached - Similar pages

> Citations: Overlapped Loop Support in the Cydra - Dehnert, Hsu ...
> Improved **Spill** Code Generation for Software Pipelined. ... A **rotating register** file can be used to solve this problem without replicating code by renaming ...
> citeseer.ist.psu.edu/context/49619/0 - 37k - Cached - Similar pages
> [More results from citeseer.ist.psu.edu]

Method, apparatus, and product for optimizing compiler with ...
(i) when the second **rotating register** is not available, inserting one or more **spill** code instructions in the first IR for the second live range, and ...
www.freepatentsonline.com/6651247.html - 149k - Cached - Similar pages

Register Constrained Modulo Scheduling
A **rotating register** file can be used to solve this problem without replicating ... This is accomplished by scheduling the **spill** operation and its associated ...
doi.ieeecomputersociety.org/10.1109/TPDS.2004.1278099 - Similar pages

[PDF] Itanium
File Format: PDF/Adobe Acrobat - View as HTML
stack frame and **rotating register** base for GRs. The CFM holds the ... perform **register spill** and reload operations in the background when neces- ...
www.cse.unsw.edu.au/~cs9244/06/seminars/07-gaol.pdf - Similar pages

[PPT] IA-64 Architecture Innovations
File Format: Microsoft Powerpoint - View as HTML
Exposes **register** renaming to SW; Avoids **register spill** when few needed ... Separate **Rotating Register** Base for each: GRs, FRs, PRs; Loop branches decrement ...
www.es.ele.tue.nl/~heco/courses/aca/IA64/dale.ppt - Similar pages

HP OpenVMS systems documentation
The **rotating register** region always starts with R32, and may be any multiple ... This allows a procedure to **spill** its **register** parameters easily to memory ...
h71000.www7.hp.com/DOC/82FINAL/5841/5841pro_053.html - 45k - Cached - Similar pages

An Overview of the Intel IA-64 Compile
In IA-64, **rotating** predicates [5, 6, 7] are used to control the execution ... a basic block and is run after **register** allocation to schedule the **spill** code. ...
developer.intel.com/technology/itj/q41999/articles/art_1k.htm - 16k - Cached - Similar pages

CCCP: Trimaran Compiler Framework
... hardware support like predicates and **rotating register** files. ... coloring based **register** allocation algorithm. **Spill** code is introduced if necessary. ...

lloth.eecs.umich.edu/research/trimaran.php - 7k - Cached - Similar pages

Gooooooooogle ▶

Result Page: 1 2 3 4 5 6 7 8 9 10 **Next**

---

rotating register spill Search

Search within results | Language Tools | Search Tips | Dissatisfied? Help us improve

---

Web Results **1** - **10** of about **502,000** for **floating point register spill**. (**0.39** seconds)

[PDF] How Futile are Mindless Assessments of Roundoff in **Floating-Point** ...
File Format: PDF/Adobe Acrobat - View as HTML
Hardware conforming to IEEE Standard 754 for Binary **Floating-Point** does ... Sometimes compilers "**spill**" the contents of a wide **register** temporarily to a ...
www.cs.berkeley.edu/~wkahan/Mind1ess.pdf - Similar pages

ia64 **floating point** - GCC Wiki
The ia64 architecture's **floating point** has a number of exotic features: ... 'fill/**spill**' instructions that transfer the complete internal **register** content. ...
gcc.gnu.org/wiki/ia64%20**floating**%20**point** - 30k - Cached - Similar pages

Re: **FLOATING-POINT** CONSISTENCY, -FFLOAT-STORE, AND X86
Re: **FLOATING-POINT** CONSISTENCY, -FFLOAT-STORE, AND X86 ... but there was no efficient way to **spill** the full **register** width, nor would there have been much ...
gcc.gnu.org/ml/gcc/1998-12/msg00097.html - 13k - Cached - Similar pages
[More results from gcc.gnu.org]

Register Allocation
The integer and **floating point register** allocators are functors that only take client ... **spill**/reload: are functions that describe how to **spill** and reload ...
cs.nyu.edu/leunga/www/MLRISC/Doc/html/mlrisc-ra.html - 12k - Cached - Similar pages

[LLVMbugs] [Bug 467] NEW: [X86] **Spill floating point** stack values ...
GCC takes the position that X86 **floating point** is already hopeless: many optimizations (eg **register** promotions, store-load forwarding, etc) hopelessly ...
lists.cs.uiuc.edu/pipermail/llvmbugs/2004-December/000972.html - 5k - Cached - Similar pages

Register Allocation
The results show that the **spill** heuristics and scratch **register** ... Mtrt degrades as we add more optimizations; however, the **floating-point** results here ...
www.usenix.org/event/jvm02/full_papers/alpern/alpern_html/node15.html - 11k - Cached - Similar pages

Lecture 4- CSC/MA 783 --Gary Howell Optimizing In-Cache **Floating** ...
This appears to because we had **register spill** so that only about half of the instructions were **floating point** adds and multiplies (the rest being loads back ...
www.ncsu.edu/itd/hpc/Courses/4incache.html - 15k - Cached - Similar pages

Andrew Cagney - Re: MIPS o32 ABI spec, $fp1 valid?
Does the o32 ABI specify how to **spill** a loating **point register** (a **spill** is ... Each even/odd pair of the 32 **floating-point** general registers can be used as ...
www.sourceware.org/ml/gdb/2003-06/msg00334.html - 7k - Cached - Similar pages

[PDF] Microsoft PowerPoint - lecture16 prn
File Format: PDF/Adobe Acrobat - View as HTML
Register set depends on the data-type. – **floating-point** values in **floating point** registers ... **Spill** the value to memory and load it back at the ...
web.mit.edu/6.035/www/slides-2005/**Register**Allocation.pdf - Similar pages

HP OpenVMS systems documentation
The argument item sequence can have a mix of integer and **floating-point** items ... This allows a procedure to **spill** its **register** parameters easily to memory ...

h71000.www7.hp.com/DOC/82FINAL/5841/5841pro_053.html - 45k -
Cached - Similar pages

Goooooooooogle ▶

Result Page: 1 2 3 4 5 6 7 8 9 10 **Next**

floating point register spill Search

Search within results | Language Tools | Search Tips | Dissatisfied? Help us improve

Google Home - Advertising Programs - Business Solutions - About Google

Sign in

Google

Web Images Video[New!] News Maps more »

register allocation Search Advanced Search Preferences

Web

Results 1 - 10 of about 21,300,000 for register allocation. (0.37 seconds)

Register allocation - Wikipedia, the free encyclopedia
In compiler optimization, **register allocation** is the process of multiplexing a large ...
Register allocation can happen over a basic block (local **register** ...
en.wikipedia.org/wiki/**Register_allocation** - 17k - Cached - Similar pages

Register Allocation
One very active application for graph coloring is **register allocation**. The **register allocation** problem is to assign variables to a limited number of ...
mat.gsia.cmu.edu/COLOR/general/ccreview/node5.html - 3k - Cached - Similar pages

[PDF] Linear Scan **Register Allocation**
File Format: PDF/Adobe Acrobat - View as HTML
We describe a global **register allocation** algorithm, called linear scan, ... This section evaluates linear scan **register allocation** in terms of both compile- ...
www.cs.ucla.edu/~palsberg/course/cs132/linearscan.pdf - Similar pages

12.1 **Register Allocation** Using the Interference Graph
12.1 **Register Allocation** Using the Interference Graph.
lambda.uta.edu/cse5317/notes/node42.html - 10k - Cached - Similar pages

12 **Register Allocation**
12 **Register Allocation**. ... Subsections. 12.1 **Register Allocation** Using the Interference Graph · 12.2 Code Generation for Trees ...
lambda.uta.edu/cse5317/notes/node41.html - 3k - Cached - Similar pages

A Generalized Algorithm for Graph-Coloring **Register Allocation** ...
Graph-coloring **register allocation** is an elegant and extremely popular ... We present a generalization of graph-coloring **register allocation** that handles ...
www.eecs.harvard.edu/nr/pubs/gcra-abstract.html - 2k - Cached - Similar pages

Linear Scan **Register Allocation** - Poletto, Sarkar (ResearchIndex)
This article we use depth first order. The choice of instruction ordering does not a ect the correctness of the algorithm, but it may a ect the quality of ...
citeseer.ist.psu.edu/poletto99linear.html - 25k - Cached - Similar pages

Register Allocation via Graph Coloring - Briggs (ResearchIndex)
Chaitin and his colleagues at IBM in Yorktown Heights built the first global **register** allocator based on graph coloring. This thesis describes a series of ...
citeseer.ist.psu.edu/briggs92**register**.html - 32k - Cached - Similar pages
[More results from citeseer.ist.psu.edu]

[PDF] THESIS **REGISTER ALLOCATION** AND ASSIGNMENT IN A RETARGETABLE ...
File Format: PDF/Adobe Acrobat - View as HTML
This section will discuss several methods of **register allocation** and assignment: ... **Register allocation** and spilling via graph coloring. In Proceedings of ...
emess.mscd.edu/~beaty/Dossier/Papers/thesis.pdf - Similar pages

Differential **register allocation**

We demonstrate that differential **register allocation** is helpful in improving ... 16 BR Rau ,

M. Lee , PP Tirumalai , MS Schlansker, **Register allocation** for ...
portal.acm.org/citation.cfm?id=1065031&
dl=acm&coll=&CFID=15151515&CFTOKEN=6184618 - Similar pages

Goooooooooogle ▶

Result Page: 1 2 3 4 5 6 7 8 9 10 **Next**